IN THE CLAIMS:

Please cancel claims 5, 16, 19-21, and amend the claims as follows:

1. (Currently Amended) A method for testing memory cells of a DRAM memory chip arranged together with a non-volatile memory chip in a multichip memory module incorporated in an application apparatus, comprising:

conducting a self-test of the memory cells of the DRAM memory chip in a time period during which the memory cells of the DRAM memory chip are not accessed in an ~~operative~~ operating mode of the application apparatus;

providing signals, utilizing a self-test control device located within the DRAM memory chip to a control input of the DRAM memory chip and a control input at the nonvolatile memory chip; and

disconnecting control input signals from outside the multichip memory module using the self-test control device.

2. (Original) The method of claim 1, further comprising:

initiating the self-test by a central processing unit of the application apparatus, the central processing unit arranged outside the multichip memory module.

3. (Original) The method of claim 1, wherein a data bus of the DRAM memory chip and a data bus of the nonvolatile memory chip are connected, further comprising:

storing addresses of defective memory cells in the nonvolatile memory chip.

4. (Original) The method of claim 3, further comprising:

deactivating, utilizing a switching device, a common data bus of the DRAM memory chip and the nonvolatile memory chip disposed outside the multichip memory module.

5. (Canceled) The method of claim 1, further comprising:

providing signals, utilizing a self-test control device, to a control input of the DRAM memory chip and a control input at the nonvolatile memory chip; and

disconnecting control input signals from outside the multichip memory module.

6. (Original) The method of claim 1, further comprising:

selecting addresses of the DRAM memory chip to test memory cells utilizing a self-test control device disposed in the DRAM memory chip.

7. (Original) The method of claim 3, further comprising:

selecting addresses of the nonvolatile memory chip to store the addresses of the defective memory cells of the DRAM memory chip utilizing a central processing unit.

8. (Currently Amended) The method of claims 7, wherein the addresses of the defective memory cells are read from the nonvolatile memory chip by the central processing unit in the ~~operative~~ operating mode of the application apparatus.

9. (Currently Amended) The method of claim 8, wherein the addresses of the defective memory cells are skipped by an address decoding circuit of the DRAM memory chip during the ~~operative~~ operating mode of the application apparatus.

10. (Original) The method of claim 1, further comprising:

replacing defective memory cells identified by the self-test with redundant memory cells in the DRAM memory chip.

11. (Original) The method of claim 1, wherein the self-test is conducted in a period from at least one of:

during a battery charging period of the application apparatus;
during a standby period of the application apparatus;
after a battery change of the application apparatus;
after an initial switch-on of the application apparatus;
after a switch-off of the application apparatus; and
according to a time schedule stored in the nonvolatile memory chip.

12. (Currently Amended) An apparatus for testing memory cells of a DRAM memory chip disposed with a nonvolatile memory chip in a multichip memory module incorporated in an application apparatus, comprising:

a self-test control device, disposed in one of the DRAM memory chip and the nonvolatile memory chip, for conducting a self-test of the memory cells of the DRAM

memory chip in a time period during which the memory cells of the DRAM memory chip are not accessed in an ~~operative~~ operating mode of the application apparatus; and

a second switching device for disconnecting the control inputs at the DRAM memory chip and at the nonvolatile memory chip from outside the multichip memory module; and wherein the self-test control device provides signals to control inputs of the DRAM memory chip and control inputs of the nonvolatile memory chip.

13. (Original) The apparatus of claim 12, further comprising:

a central processing unit, disposed outside the multichip memory module and connected to the self-test control device, for initiating the self-test and providing control commands to the DRAM memory chip.

14. (Original) The apparatus of claim 13, wherein the multichip memory module includes a data bus of the DRAM memory chip and a data bus of the nonvolatile memory chip which are connected during the self-test to store addresses of defective memory cells in the nonvolatile memory chip.

15. (Original) The apparatus of claim 14, further comprising:

a switching device for deactivating a common data bus of the DRAM memory chip and of the nonvolatile memory chip outside the multichip memory module.

16. (Canceled) The apparatus of claim 15, further comprising a second switching device for disconnecting the control inputs at the DRAM memory chip and at the nonvolatile memory chip from outside the multichip memory module; and wherein the self-test control device provides signals to control inputs of the DRAM memory chip and control inputs of the nonvolatile memory chip.

17. (Original) The apparatus of claim 12, wherein the DRAM memory chip includes redundant memory cells for replacing defective memory cells determined by the self-test.

18. (Currently Amended) An apparatus for testing memory cells of a DRAM memory chip disposed with a nonvolatile memory chip in a multichip memory module incorporated in an application apparatus, comprising:

a self-test control means, disposed in one of the DRAM memory chip and the nonvolatile memory chip, for conducting a self-test of the memory cells of the DRAM memory chip in a time period during which the memory cells of the DRAM memory chip are not accessed in an ~~operative~~ operating mode of the application apparatus;

a central processing means, disposed outside the multichip memory module and connected to the self-test control device, for initiating the self-test and providing control commands to the DRAM memory chip;

a switching means for deactivating a common data bus of the DRAM memory chip and of the nonvolatile memory chip outside the multichip memory module; and wherein the multichip memory module includes a data bus of the DRAM memory chip and a data bus of the nonvolatile memory chip which are connected during the self-test to store addresses of defective memory cells in the nonvolatile memory chip; and

a second switching means for disconnecting the control inputs at the DRAM memory chip and at the nonvolatile memory chip from outside the multichip memory module; and wherein the self-test control means provides signals to control inputs of the DRAM memory chip and control inputs of the nonvolatile memory chip.

19. (Canceled) The apparatus of claim 18, further comprising:

a central processing means, disposed outside the multichip memory module and connected to the self-test control device, for initiating the self-test and providing control commands to the DRAM memory chip.

20. (Canceled) The apparatus of claim 19, further comprising a switching means for deactivating a common data bus of the DRAM memory chip and of the nonvolatile memory chip outside the multichip memory module; and wherein the multichip memory module includes a data bus of the DRAM memory chip and a data bus of the nonvolatile memory chip which are connected during the self-test to store addresses of defective memory cells in the nonvolatile memory chip.

21. (Canceled) The apparatus of claim 20, further comprising a second switching means for disconnecting the control inputs at the DRAM memory chip and at the nonvolatile memory chip from outside the multichip memory module; and wherein the

self-test control means provides signals to control inputs of the DRAM memory chip and control inputs of the nonvolatile memory chip.